What is claimed is:

1.   A method comprising:

    translating a design description into configurations for a plurality of processing elements on a single integrated circuit; and

    setting at least one packet size for packet communications between the plurality of processing elements on the single integrated circuit.

2.   The method of claim 1 wherein translating comprises partitioning the design into a plurality of functions.

3.   The method of claim 2 wherein translating further comprises compiling the plurality of functions to code to run on at least one of the plurality of processing elements.

4.   The method of claim 1 further comprising profiling a design represented by the configurations for the plurality of processing elements.

5.   The method of claim 4 further comprising changing a power supply voltage value in response to the profiling.

6.   The method of claim 4 further comprising changing a clock frequency in response to the profiling.

7.   The method of claim 4 further comprising changing the at least one packet size in response to the profiling.

8.   The method of claim 4 wherein profiling produces information describing latency.

1   9.   The method of claim 4 wherein profiling produces information describing
2   throughput.

1   10.   The method of claim 4 further comprising comparing user constraints with
2   output from the profiling.

1   11.   The method of claim 10 wherein the user constraints include latency.

1   12.   The method of claim 10 wherein the user constraints include throughput.

1   13.   The method of claim 4 further comprising modifying parameters of the
2   processing elements in response to the profiling.

1   14.   A method comprising:
2   dividing a design description into a plurality of functions;
3   compiling at least one function into machine code to run on a first
4   processing element;
5   translating at least one other function into a configuration for a second
6   processing element; and
7   setting a packet size for packet communications between the first and second
8   processing elements.

1   15.   The method of claim 14 further comprising generating configuration packets
2   to configure an integrated circuit that includes the first and second processing
3   elements.

1   16.   The method of claim 15 further comprising configuring the integrated circuit
2   with the configuration packets.

1   17.   The method of claim 14 wherein translating at least one other function
2   comprises translating a plurality of other functions into a configuration for the
3   second processing element.

1   18.   The method of claim 14 further comprising profiling a design with the
2   configuration packets.

1   19.   The method of claim 18 further comprising modifying the packet size in
2   response to the profiling.

1   20.   The method of claim 18 further comprising modifying a power supply
2   voltage of the first processing element in response to the profiling.

1   21.   The method of claim 18 further comprising modifying a power supply
2   voltage of the second processing element in response to the profiling.

1   22.   The method of claim 18 further comprising modifying a clock frequency of
2   the first processing element in response to the profiling.

1   23.   The method of claim 18 further comprising modifying a clock frequency of
2   the second processing element in response to the profiling.

1   24.   An apparatus including a medium to hold machine-accessible instructions
2   that when accessed result in a machine performing:
3   reading a design description;
4   compiling the design description to configure a plurality of processing
5   elements; and
6   determining a packet size for communications between at least two of the
7   plurality of processing elements.

1   25.   The apparatus of claim 24 wherein the machine-accessible instructions when
2   accessed further result in the machine performing:
3   profiling the design; and
4   modifying at least one parameter in response to the profiling.

1   26.   The apparatus of claim 25 wherein modifying at least one parameter
2   comprises modifying a clock rate of at least one of the plurality of processing
3   elements.

1   27.   The apparatus of claim 25 wherein modifying at least one parameter
2   comprises modifying the packet size.

1   28.   An electronic system comprising:
2   a processing element; and
3   a static random access memory to hold instructions that when accessed result
4   in the processing element performing reading a design description, compiling the
5   design description to configure a plurality of processing elements, and determining a
6   packet size for communications between at least two of the plurality of processing
7   elements.

1   29.   The electronic system of claim 28 wherein the instructions when accessed
2   further result in the processing element performing profiling the design, and
3   modifying at least one parameter in response to the profiling.

1   30.   The electronic system of claim 29 wherein modifying at least one parameter
2   comprises modifying the packet size.